## Pipeline components

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| **Pipeline Register** | **Components** | **Length(bits)** |
| IFID | PC | 16 |
| Instruction | 16 |
| PC++ | 16 |
| IDRR | PC | 16 |
| SEPC | 16 |
| SE | 16 |
| CL(Control Lines) | 11 |
| * LS\_PC * BEQ * LM * LW * SE\_DO2 * WB\_mux * valid | 1  1  1  1  1  3  3 |
| Opcode | 4 |
| ALU Control | 2 |
| Flag Control | 3 |
| Condition bits | 2 |
| Write Bits | 2 |
| AR1 | 3 |
| AR2 | 3 |
| AR3 | 3 |
| PC++ | 16 |
| LM input | 8 |
| BLUT(Branch Table) | 4 |
| RREX | PC | 16 |
| LSPC | 16 |
| SE | 16 |
| CL(Control Lines) | 12 |
| * BEQ * LW * SE\_DO2 * WB\_mux * Valid * LM\_SM control | 1  1  1  3  3  3 |
| ALU Control | 2 |
| Flag Control | 3 |
| Condition | 2 |
| Write | 2 |
| BLUT | 4 |
| DO1 | 16 |
| DO2 | 16 |
| AR1 | 3 |
| AR2 | 3 |
| AR3 | 3 |
| PC++ | 16 |
| EXMM | LSPC | 16 |
| SE | 16 |
| CL(Control Lines) | 8 |
| * BEQ * WB\_mux * Valid * LM\_SM control | 1  3  3  1 |
| Flag Control | 3 |
| Condition | 2 |
| Write | 2 |
| AR1 | 3 |
| AR2 | 3 |
| AR3 | 3 |
| Flags | 3 |
| DO1 | 16 |
| DO2 | 16 |
| ALU output | 16 |
| MMWB | LSPC | 16 |
| SE | 16 |
| CL(Control Lines) | 7 |
| * BEQ * WB\_mux * valid | 1  3  3 |
| Flag Control | 3 |
| Condition | 2 |
| Write | 2 |
| AR1 | 3 |
| AR2 | 3 |
| AR3 | 3 |
| ALU output | 16 |
| Memory output | 16 |
| DO1 | 16 |
| PC++ | 16 |